

In the Claims:

Please amend claims 1-10, and add new claims 14-20 as indicated below. This listing of claims replaces all prior versions.

1. (Currently amended) A digital to analog converter comprising a first current source ~~(3)~~ connected to a plurality of common lines ~~(20,21)~~ and to a first node ~~(23,36)~~, wherein said first node ~~(23,36)~~ forms an output of the digital to analog converter via a ~~respective~~ first switch ~~(35,38,46)~~ whose state is controlled in accordance with a first applied digital signal ~~(28,31)~~ to be converted, the first applied digital signal occurring at substantially irregular intervals, the digital to analog converter further comprising a second current source ~~(30)~~ which is associated with said first current source ~~(3)~~, wherein said second current source ~~(30)~~ is connected to at least one of said common lines ~~(20,21)~~ and to a second node ~~(26,37)~~ via a ~~respective~~-second switch ~~(39)~~ whose state is controlled in accordance with a second applied digital signal ~~(29,32)~~, characterized in that the second applied digital signal ~~(29,32)~~ causes said second ~~respective~~ switch ~~(39)~~ to change state such that influences on the at least said one of said common lines ~~(20,21)~~-caused by said first and second switches ~~(38,39)~~ switching ~~are periodic~~ occur at substantially regular intervals.
2. (Currently amended) A digital to analog converter according to claim 1, wherein said first signal ~~(28,31)~~ ~~comprises~~ has a plurality of signal components ~~(41-46)~~ each having a duration substantially equal to one or more clock cycles, and wherein said second signal ~~(29,32)~~ is derived from said first signal ~~(28,31)~~ so that, during data conversion, during ~~any one~~ each clock cycle ~~either said first current source ~~(3)~~ or said associated second current source ~~(30)~~~~ one and only one of the first and second switches is caused to switch.
3. (Currently amended) A digital to analog converter according to claim 1, further comprising a power supply ~~(9)~~ to which said first current source ~~(3)~~ and said second current source are connected ~~(30)~~.

4. (Currently amended) A digital to analog converter according to claim 1, wherein said first current source ~~(3)~~ is disposed adjacent to said second associated current source ~~(30)~~.
5. (Currently amended) A digital to analog converter according to claim 1, wherein said first and second digital signals ~~(31,32)~~ are carried on first and second digital input lines ~~(28,29)~~, respectively, wherein said first digital input line ~~(28)~~ is connected to said first switch ~~(38)~~ and said second digital input line ~~(29)~~ is connected to said second switch ~~(39)~~, wherein said first and second digital input lines ~~(28,29)~~ are arranged in parallel.
6. (Currently amended) A digital to analog converter according to claim 1, wherein said second digital signal ~~(32)~~ is generated by a signal generating means ~~(10)~~ comprising a circuit for identifying clock cycles in said first digital signal ~~(31)~~ in which, when applied to said first switch ~~(38)~~, a signal component causes said first current source ~~(3)~~ to switch, and for generating in response to the identification, a second digital signal ~~(32)~~ including a signal component which, when applied to said second switch ~~(39)~~, causes said second current source ~~(30)~~ to switch, in those clock cycles in which no such component is identified in said first digital signal ~~(31)~~, so that, during data conversion, in any one each clock cycle, either said first or said second current source ~~(3,30)~~ one of the first and second switches is caused to switch.
7. (Currently amended) A digital to analog converter according to claim 1, wherein output loads associated with the first and second nodes ~~(23,36,26,37)~~ are substantially matched.
8. (Currently amended) A digital to analog converter according to claim 1, further comprising a plurality of first current sources ~~(3,5,7)~~, each of which is associated with one of a plurality of second current sources ~~(30,50,70)~~, wherein each of said plurality of first and second current sources ~~(3,30,5,50,7,70)~~ is provided with a respective switch ~~(39)~~.

9. (Currently amended) A method of converting a digital signal to an analog signal comprising the steps of:
- providing a first current source (3),
 - connecting said first current source (3) to a plurality of common lines (20,21) and to a first node (23,36), wherein said first node (23,36) forms an output of the digital to analog converter via a ~~plurality of respective first switches (38)~~ whose states ~~are is~~ controlled in accordance with a first applied digital signal (28,31) to be converted, the first applied digital signal occurring at substantially irregular intervals,
 - further providing a second current source (30) which is associated with said first current source (3), connecting said second current source (30) to at least one of said common lines (20,21) and to a second node (26,37) via a ~~respective second current switch (39)~~ whose state is controlled in accordance with a second applied digital signal (29,32) characterized by applying said second digital signal (29,32) to said second ~~respective switch (39)~~ causing said ~~respective second switch (39)~~ to change state such that influences on the at least ~~said~~ one of said common lines (20,21) caused by said first and second switches (38,39) ~~switching are periodic~~ occur at substantially regular intervals.
10. (Currently amended) A digital to analog converter according to claim 1 wherein said second current source (30) is identical to said first current source (3).
11. (Previously presented) A digital to analog converter according to claim 7 wherein said output loads are components that register an output signal and put a load on the output nodes of the digital to analog converter.
12. (Previously presented) A digital to analog converter according to claim 7 wherein said output loads are a cable line.
13. (Previously presented) A digital to analog converter according to claim 7 wherein said output loads are an antenna.

14. (New) A digital to analog converter comprising:

a first current source connected to a plurality of common lines and to a first node, the first node forming an output of the digital to analog converter via a first switch whose state is controlled in accordance with a first applied digital signal to be converted, the first applied digital signal having a plurality of signal components each having a duration substantially equal to one or more clock cycles; and

a second current source that is associated with the first current source, the second current source connected to at least one of the common lines and to a second node via a second switch whose state is controlled in accordance with a second applied digital signal, the second applied digital signal derived from the first applied digital signal such that, during data conversion, during any one clock cycle either the first current source or the associated second current source is caused to switch;

characterized in that the second applied digital signal causes the second switch to change state such that influences on the at least one common line caused by the first and second switches switching are periodic.

15. (New) A digital to analog converter according to claim 14, further comprising a power supply to which said first current source and said second current source are connected.

16. (New) A digital to analog converter according to claim 14, wherein said first current source is disposed adjacent to said second associated current source.

17. (New) A digital to analog converter according to claim 14, wherein said first and second digital signals are carried on first and second digital input lines, respectively, the first and second digital input lines arranged in parallel, and wherein said first digital input line is connected to said first switch and said second digital input line is connected to said second switch.

18. (New) A digital to analog converter according to claim 14, wherein said second digital signal is generated by signal generating means comprising a circuit for identifying clock cycles in said first digital signal in which, when applied to said first switch, a signal component causes said first current source to switch, and for generating in response to the identification, the second digital signal including a signal component which, when applied to said second switch, causes said second current source to switch, in those clock cycles in which no such component is identified in said first digital signal, so that, during data conversion, in any one clock cycle, either said first or said second current source is caused to switch.

19. (New) A digital to analog converter according to claim 14, wherein output loads associated with the first and second nodes are substantially matched.

20. (New) A digital to analog converter according to claim 14, further comprising a plurality of first current sources, each of which is associated with one of a plurality of second current sources, wherein each of the plurality of first and the plurality of second current sources is provided with a respective switch.